

CLAIMS

What is claimed is:

1. A microelectronic package, comprising:
 2. a microelectronic package core having a first surface and an opposing second surface, said microelectronic package core having at least one opening defined therein extending from said microelectronic package core first surface to said microelectronic package core second surface;
 6. at least one microelectronic die disposed within said at least one opening, said at least one microelectronic die having an active surface; and
 8. an encapsulation material adhering said microelectronic package core to said at least one microelectronic die.
1. 2. The microelectronic package of claim 1, wherein said encapsulation material further includes at least one surface substantially planar to said microelectronic die active surface and said microelectronic package core first surface.
1. 3. The microelectronic package of claim 2, further including build-up layers disposed on at least one of said microelectronic die active surface, said at least one encapsulation material surface, and said microelectronic package core first surface.
1. 4. The microelectronic package of claim 3, wherein said build-up layers comprise at least one dielectric layer abutting at least one of said microelectronic die

3 active surface, said at least one encapsulation material surface, and said microelectronic
4 package core first surface and at least one conductive trace disposed on said at least one
5 dielectric layer.

1 5. The microelectronic package of claim 4, wherein said at least one
2 conductive trace extends through said at least one dielectric layer to contact at least one
3 electrical contact on said microelectronic die active surface.

1 6. The microelectronic package of claim 1, wherein at thickness of said
2 microelectronic die is greater than a thickness of said microelectronic package core.

1 7. The microelectronic package of claim 6, wherein said microelectronic
2 package core includes at least one via extending therethrough.

1 8. The microelectronic package of claim 1, wherein said microelectronic
2 package core is selected from the group consisting of bismaleimide triazine resin based
3 material, an FR4 material, polyimides, ceramics, and metals.

1 9. A method of fabricating a microelectronic package, comprising:
2 providing a microelectronic package core having a first surface and an opposing
3 second surface, said microelectronic package core having at least one opening defined

4 therein extending from said microelectronic package core first surface to said
5 microelectronic package core second surface;
6 disposing at least one microelectronic die within said at least one opening, said at
7 least one microelectronic die having an active surface; and
8 adhering said microelectronic package core to said at least one microelectronic
9 die with an encapsulation material.

1 10. The method of claim 9, wherein adhering said microelectronic package
2 core to said at least one microelectronic with said encapsulation material further includes
3 forming at least one encapsulation material surface substantially planar to said
4 microelectronic die active surface and said microelectronic package core first surface.

1 11. The method of claim 10, further including:
2 forming at least one dielectric material layer on at least a portion of said
3 microelectronic die active surface, said at least one encapsulation material surface, and
4 said microelectronic package core first surface;
5 forming at least one via through said at least one dielectric material layer to
6 expose a portion of said microelectronic die active surface; and
7 forming at least one conductive trace on said at least one dielectric material layer
8 which extends into said at least one via to electrically contact said microelectronic die
9 active surface.

1 12. The method of claim 11, further including forming at least one additional
2 dielectric material layer disposed over said at least one conductive trace and said at least
3 one dielectric material layer.

1 13. The method of claim 12, further including forming at least one additional
2 conductive trace to extend through and reside on said at least one additional dielectric
3 material layer.

1 14. The method of claim 9, wherein said providing said microelectronic
2 package core comprises providing a microelectronic package core selected from the
3 group consisting of bismaleimide triazine resin based material, an FR4 material,
4 polyimides, ceramics, and metals.

1 15. A method of fabricating a microelectronic package, comprising:
2 providing a microelectronic package core having a first surface and an opposing
3 second surface, said microelectronic package core having at least one opening defined
4 therein extending from said microelectronic package core first surface to said
5 microelectronic package core second surface;
6 abutting a protective film against said microelectronic package core first surface,
7 wherein said protective film spans said at least one opening;

8 disposing at least one microelectronic die within said at least one opening,
9 wherein an active surface of said microelectronic die abuts a portion of said protective
10 film;

11 adhering said microelectronic package core to said at least one microelectronic
12 die with an encapsulation material, wherein a portion of said encapsulation material fills a
13 portion of said opening to form at least one encapsulation material surface abutting said
14 protective film; and

15 removing said protective film.

1 16. The method of claim 15, further including:

2 forming at least one dielectric material layer on at least a portion of said
3 microelectronic die active surface, said at least one encapsulation material surface, and
4 said microelectronic package core first surface;

5 forming at least one via through said at least one dielectric material layer to
6 expose a portion of said microelectronic die active surface; and

7 forming at least one conductive trace on said at least one dielectric material layer
8 which extends into said at least one via to electrically contact said microelectronic die
9 active surface.

1 17. The method of claim 16, further including forming at least one additional
2 dielectric material layer disposed over said at least one conductive trace and said at least
3 one dielectric material layer.

1 18. The method of claim 17, further including forming at least one additional
2 conductive trace to extend through and reside on said at least one additional dielectric
3 material layer.

1 19. The method of claim 15, wherein said providing said microelectronic
2 package core comprises providing a microelectronic package core selected from the
3 group consisting of bismaleimide triazine resin based material, an FR4 material,
4 polyimides, ceramics, and metals.

1 20. The method of claim 15, wherein said abutting said protective film
2 includes abutting said protective film having an adhesive against said microelectronic
3 package core first surface.

1 21. A method of fabricating a microelectronic package, comprising:
2 providing a microelectronic package core having a first surface and an opposing
3 second surface, said microelectronic package core having a plurality of openings defined
4 therein extending from said microelectronic package core first surface to said
5 microelectronic package core second surface;
6 abutting a protective film against said microelectronic package core first surface,
7 wherein said protective film spans said at least one opening;

8 disposing a plurality of microelectronic dice within corresponding openings of the
9 microelectronic package core, wherein active surfaces of each of said microelectronic
10 dice abuts a portion of said protective film;

11 adhering said microelectronic package core to said plurality of microelectronic
12 dice with an encapsulation material, wherein a portion of said encapsulation material fills
13 a portion of said openings to form a plurality of encapsulation material surfaces abutting
14 said protective film;

15 removing said protective film; and

16 singulating each microelectronic die by cutting through said microelectronic
17 package core.

1 22. The method of claim 21, further including:

2 forming build-up layers on at least a portion of said microelectronic dice active
3 surfaces, said plurality of encapsulation material surfaces, and said microelectronic
4 package core first surface.

1 23. The method of claim 21, wherein said providing said microelectronic
2 package core comprises providing a microelectronic package core selected from the
3 group consisting of bismaleimide triazine resin based material, an FR4 material,
4 polyimides, ceramics, and metals.

1 24. The method of claim 21, wherein abutting said protective film includes
2 abutting said protective film having an adhesive against said microelectronic package
3 core first surface.